**VisionForge**

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Due date: 31 Dec, 2023

Due time: 11:59PM

**Mini Project-1**

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Create a Verilog design for a clock with an alarm, incorporating the following features.

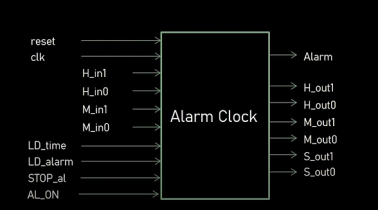
● Clock Generation

● Initializing clock time to a particular value

● Setting time for alarm

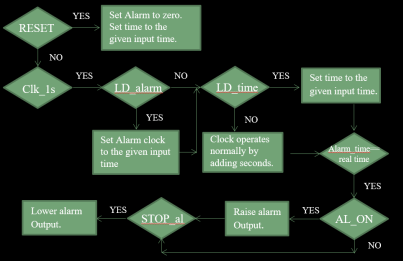
● Enabling and disabling alarm

● Stopping alarm

Presented here is the Block Diagram for the clock system 

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Here is the Flow chart illustrating the operations of the clock system

Collaborative undertake and submit this project as a group!

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